Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (new) A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first and second L-byte boundaries of said secondary memory address space; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said step of transferring, initiating a respective set of at least one snoop access of said cache memory, the snoop accesses in each set collectively specifying the respective N+1'th L-byte line in its entirety, and all the snoop accesses in each set being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective (N+1)'th L-byte line,

wherein said step of transferring comprises the step of transferring to said bus master three sequential data units including the last data unit before said first L-byte boundary and the first data unit beyond said first L-byte line, all at a constant rate,

and wherein said step of transferring further comprises the step of transferring to said bus master three sequential data units including the last data unit before said second L-byte boundary and the first data unit beyond said second L-byte line, all at a constant rate.

3. (new) A method according to claim 2, wherein said step of sequentially transferring data units continues further beyond a third L-byte boundary of said secondary memory,

and wherein said step of transferring further comprises the step of transferring three sequential data units including the last data unit before said third L-byte boundary and the first data unit beyond said third L-byte line, all at a constant rate.

4. (new) A method according to claim 2, further comprising the step of sampling the result of each of said snoop accesses prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

5. (new) A method according to claim 2, wherein said step of sequentially transferring data units comprises the steps, for each given one of said data units, of:

driving said given data unit onto a PCI bus; and

asserting a target-ready signal on said PCI bus for sampling by said bus master in dependence upon a PCI-bus clock signal.

6. (new) A method according to claim 2, wherein said processing unit samples snoop accesses in accordance with a first clock, and wherein said bus master samples data transferred to it in accordance with a PCI clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

7. (new) A method according to claim 2, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

8. (new) A method according to claim 2, wherein all the snoop accesses in each respective set of snoop accesses initiated in said step of initiating, are initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

9. (new) A method according to claim 2, wherein the set of snoop accesses collectively specifying a particular one of the L-byte lines in its entirety contains all the snoop accesses of said cache memory which are initiated in said step of transferring and which specify any part of the particular L-byte line.

10. (new) A method according to claim 2, wherein each of said sets of snoop accesses contains exactly one snoop access.

11. (new) A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first and second L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, three sequential data units bracketing said first L-byte boundary being transferred to said bus master at a constant rate, and three sequential data units bracketing said second L-byte boundary being transferred to said bus master at said constant rate, said constant rate being dependent upon the frequency of a PCI-bus clock provided to said bus master; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said step of transferring, initiating a snoop access of said cache memory, said snoop accesses specifying the respective N+1'th L-byte line in its entirety and being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective (N+1)'th L-byte line, said snoop accesses being sampled by said

processing unit in accordance with a first clock signal having a frequency that is at least twice said PCI-bus clock frequency.

12. (new) A method according to claim 11, wherein said step of sequentially transferring data units comprises the step of reading data at a constant rate for said at least three sequential data units from said secondary memory.

13. (new) A method according to claim 11, wherein the snoop access initiated in said step of initiating, is initiated early enough such that it can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

14. (new) Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst transaction initiated by said bus master,

sequentially transfers data units to said bus master from said secondary memory according to said transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first and second L-byte boundaries of said secondary memory address space; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line according to said transaction, initiates a respective set of at least one snoop access of said cache memory, the snoop accesses in each set collectively specifying the respective N+1'th L-byte line in its entirety, and said circuitry initiating all the snoop accesses in each set early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective (N+1)'th L-byte line,

wherein said transaction includes the transfer of a plurality of sequential data units bracketing said first and second L-byte boundaries,

wherein said circuitry in said mode of operation transfers said plurality of sequential data units all at a constant rate if said snoop accesses return negatively.

15. (new) Apparatus according to claim 14, wherein said plurality of sequential data units bracketing said first and second L-byte boundaries includes the second-to-last data unit before said first L-byte boundary.

16. (new) Apparatus according to claim 15, wherein said circuitry in said mode of operation further reads data from said secondary memory at a constant rate for all of the data units in said plurality of sequential data units.

17. (new) Apparatus according to claim 14, were in said circuitry in said mode of operation samples the result of each of said snoop accesses prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

18. (new) Apparatus according to claim 14, wherein said processing unit samples all snoop accesses in accordance with a first clock, and wherein said bus master samples all data transferred to it in accordance with a PCI clock, and wherein in said mode of operation said first clock operates at at least twice the frequency of said PCI clock.

19. (new) Apparatus according to claim 14, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

20. (new) Apparatus according to claim 14, wherein all the snoop accesses in each respective set of snoop accesses initiated in said step of initiating, are initiated by said circuitry in said mode of operation early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

21. (new) Apparatus according to claim 14, wherein the set of snoop accesses collectively specifying a particular one of the L-byte lines in its entirety contains all the snoop accesses of said cache memory which are initiated by said circuitry for said transaction and which specify any part of the particular L-byte line.

22. (new) A method according to claim 14, wherein each of said sets of snoop accesses contains exactly one snoop access.

23. (new) Apparatus according to claim 14, further comprising said secondary memory, said bus master, said processing unit and said cache memory.

24. (new) Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst transaction initiated by said bus master,

sequentially transfers data units to said bus master from said secondary memory according to said PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing beyond at least first, second and third L-byte boundaries of said secondary memory address space, each full L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, a plurality of sequential data units bracketing at least said first, second and third L-byte boundaries being transferred to said bus master at a constant rate, said constant rate being dependent upon the frequency of a PCI-bus clock provided to said bus master; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line according to said transaction, initiates a snoop access of said cache memory, said snoop access specifying the respective N+1'th L-byte line in its entirety and being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective (N+1)'th L-byte line, said snoop accesses being sampled by said processing unit in accordance with a first clock signal having a frequency that is at least twice said PCI-bus clock frequency.

25. (new) Apparatus according to claim 24, wherein said circuitry further reads data from said secondary memory at a constant rate for said plurality of sequential data units bracketing at least said first, second and third L-byte boundaries.

26. (new) Apparatus according to claim 24, wherein the snoop access initiated in said step of initiating, is initiated early enough by said circuitry such that it can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

27. (new) A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through at least first and second entire L-byte lines of said secondary memory address space, said second L-byte line being transferred to said bus master in a number T_2 PCI-bus clock cycles; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said step of transferring, initiating a respective set of at least one snoop access of said cache memory, the snoop accesses in each set collectively specifying the entire respective N+1'th L-byte line, and all the snoop accesses in each set being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective (N+1)'th L-byte line,

wherein the earliest snoop access in the set of snoop accesses collectively specifying a third L-byte line, is initiated for sampling by said processing unit no more than T_2 PCI-bus clock cycles after the earliest snoop access in the set of snoop accesses collectively specifying the second L-byte line is sampled by said processing unit.

28. (new) A method according to claim 27, wherein said PCI-bus burst transaction continues at least through a third entire L-byte line of said second memory address space following said second L-byte line, said third L-byte line being transferred to said bus master in a number T_3 PCI-bus clock cycles,

and wherein the earliest snoop access in the set of snoop accesses initiated during the transfer of said third L-byte line is initiated for sampling by said processing unit no more than T_3 PCI-bus clock cycles after the earliest snoop access in the set of snoop accesses initiated during the transfer of said second L-byte line is sampled by said processing unit.

29. (new) A method according to claim 27, wherein the step of transferring comprises the step of transferring all data units of said PCI-bus burst transaction to said bus master at a constant data rate.

30. (new) A method according to claim 27, further comprising the step of sampling the result of each of said snoop accesses prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

31. (new) A method according to claim 27, wherein said step of sequentially transferring data units comprises the steps, for each given one of said data units, of:

driving said given data unit onto a PCI bus; and

asserting a target-ready signal on said PCI bus for sampling by said bus master in dependence upon a PCI-bus clock signal.

32. (new) A method according to claim 27, wherein said processing unit samples snoop accesses in accordance with a first clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

33. (new) A method according to claim 27, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

34. (new) A method according to claim 27, wherein all the snoop accesses in each respective set of snoop accesses initiated in said step of initiating, are initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

35. (new) A method according to claim 27, wherein the set of snoop accesses collectively specifying a particular one of the L-byte lines in its entirety contains all the snoop accesses of said cache memory which are initiated in said step of transferring and which specify any part of the particular L-byte line.

36. (new) A method according to claim 27, wherein each of said sets of snoop accesses contains exactly one snoop access.

37. (new) A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through a plurality of entire L-byte lines of said secondary memory address space, each L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, each entire N'th L-byte line being transferred to said bus master in a respective number T_N PCI-bus clock cycles; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said step of transferring, initiating a snoop access of said cache memory, said snoop accesses each specifying the respective N+1'th L-byte line,

wherein at least after completion of the transfer of one entire L-byte line, each snoop access specifying an N+1'th L-byte line which is not preceded by a writeback, is initiated for sampling by said processing unit no more than T_N PCI-bus clock cycles after the snoop access specifying the N'th L-byte line is sampled by said processing unit.

38. (new) A method according to claim 37, wherein each of the entire L-byte lines of the PCI-burst transaction are transferred to said bus master in an equal number T PCI-bus clock cycles.00

39. (new) A method according to claim 37, wherein said processing unit samples snoop accesses in accordance with a first clock operating at at least twice the frequency of said PCI clock, further comprising the step of sampling the result of each of said snoop accesses prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line,

and wherein the step of sequentially transferring data units comprises the step of transferring all data units of said PCI-bus burst transaction to said bus master at a constant data rate, and further comprises the steps of, for each given one of said data units:

driving said given data unit onto a PCI bus; and

asserting a target-ready signal on said PCI bus for sampling by said bus master in dependence upon a PCI-bus clock signal.

40. (new) A method according to claim 39, wherein said step of sequentially transferring data units further comprises the step of reading all data units of said PCI-bus burst transaction from said secondary memory at a constant rate.

41. (new) A method according to claim 37, wherein the snoop accesses initiated in said step of initiating, are each initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

42. (new) Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst read access initiated by said bus master,

sequentially transfers data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through at least first and second entire L-byte lines of said secondary memory address space, said second L-byte line being transferred to said bus master in a number T_2 PCI-bus clock cycles; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line, initiates a respective set of at least one snoop access of said cache memory, the snoop accesses in each set collectively specifying the entire respective N+1'th L-byte line, and all the snoop accesses in each set being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective (N+1)'th L-byte line,

wherein the earliest snoop access in the set of snoop accesses collectively specifying a third L-byte line, is initiated for sampling by said processing unit no more than T_2 PCI-bus clock cycles after the earliest snoop access in the set of snoop accesses collectively specifying the second L-byte line is sampled by said processing unit.

43. (new) Apparatus according to claim 42, wherein said PCI-bus burst transaction continues at least through a third entire L-byte line of said second memory address space following said second L-byte line, said third L-byte line being transferred to said bus master in a number T_3 PCI-bus clock cycles,

and wherein the earliest snoop access in the set of snoop accesses initiated during the transfer of said third L-byte line is initiated for sampling by said processing unit no more than T_3 PCI-bus clock cycles after the earliest snoop access in the set of snoop accesses initiated during the transfer of said second L-byte line is sampled by said processing unit.

44. (new) Apparatus according to claim 42, wherein all data units of said PCI-bus burst transaction are transferred to said bus master at a constant data rate.

45. (new) Apparatus according to claim 42, wherein said controller apparatus, in said mode of operation, further samples the result of each of said snoop accesses prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

46. (new) Apparatus according to claim 42, wherein said controller apparatus, in said mode of operation, when sequentially transferring data units, for each given one of said data units:

drives said given data unit onto a PCI bus; and

asserts a target-ready signal on said PCI bus for sampling by said bus master in dependence upon a PCI-bus clock signal.

47. (new) Apparatus according to claim 42, wherein said processing unit samples snoop accesses in accordance with a first clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

48. (new) Apparatus according to claim 42, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

49. (new) Apparatus according to claim 42, wherein all the snoop accesses in each respective set of snoop accesses initiated in said step of initiating, are initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

50. (new) Apparatus according to claim 42, wherein the set of snoop accesses collectively specifying a particular one of the L-byte lines in its entirety contains all the snoop accesses of said cache memory which are initiated in said step of transferring and which specify any part of the particular L-byte line.

51. (new) Apparatus according to claim 42, wherein each of said sets of snoop accesses contains exactly one snoop access.

52. (new) Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst read access initiated by said bus master,

sequentially transfers data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through a plurality of entire L-byte lines of said secondary memory address space, each L-byte line of said transaction requiring at least 8 data unit transfers to said bus master, each entire N'th L-byte line being transferred to said bus master in a respective number T_N PCI-bus clock cycles; and

no earlier than the transfer of the first data unit for each entire N'th L-byte line, initiates a snoop access of said cache memory, said snoop accesses each specifying the respective N+1'th L-byte line,

wherein at least after completion of the transfer of one entire L-byte line, each snoop access specifying an N+1'th L-byte line which is not preceded by a writeback, is initiated for sampling by said processing unit no more than T_N PCI-bus clock cycles after the snoop access specifying the N'th L-byte line is sampled by said processing unit.

53. (new) Apparatus according to claim 52, wherein each of the entire L-byte lines of the PCI-burst transaction are transferred to said bus master in an equal number T PCI-bus clock cycles.00

54. (new) Apparatus according to claim 52, wherein said processing unit samples snoop accesses in accordance with a first clock operating at at least twice the frequency of said PCI clock, and wherein the results of each of said snoop access are sampled prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line,

and wherein all data units of said PCI-bus burst transaction to said bus master at a constant data rate, except for any writeback delays.

55. (new) Apparatus according to claim 54, wherein said controller apparatus circuitry, in said mode of operation, reads all data units of said PCI-bus burst transaction from said secondary memory at a constant rate.

56. (new) Apparatus according to claim 52, wherein the snoop accesses initiated in said step of initiating, are each initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective N'th L-byte line.

57. (new) A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through at least three entire L-byte lines of said secondary memory address space; and

for each entire L-byte line of said transaction, initiating a respective set of at least one snoop access of said cache memory, the snoop accesses in each set collectively specifying a respective L-byte line in its entirety, all of the snoop accesses in each set being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective specified L-byte line, the first data unit of said transaction being read from said secondary memory before any snoop access specifying any part of an L-byte line beyond the first entire L-byte line of said transaction is initiated,

wherein except at cache line boundaries preceding cache lines for which a snoop access returns negatively, all data units of said PCI-bus burst transaction are transferred to said bus master at a constant data rate.

58. (new) A method according to claim 57, wherein said step of sequentially transferring data units comprises the steps, for each given one of said data units, of:

driving said given data unit onto a PCI bus; and

asserting a target-ready signal on said PCI bus for sampling by said bus master in dependence upon a PCI-bus clock signal.

59. (new) A method according to claim 58, wherein said processing unit samples snoop accesses in accordance with a first clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

60. (new) A method according to claim 57, wherein said processing unit samples snoop accesses in accordance with a first clock, and wherein said bus master samples data transferred to it in accordance with a PCI clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

61. (new) A method according to claim 57, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

62. (new) A method according to claim 57, wherein all the snoop accesses in each respective set of snoop accesses initiated in said step of initiating, are initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective L-byte line immediately preceding the specified L-byte line.

63. (new) A method according to claim 57, wherein the set of snoop accesses collectively specifying a particular one of the L-byte lines in its entirety contains all the snoop

accesses of said cache memory which are initiated in said step of transferring and which specify any part of the particular L-byte line.

64. (new) A method according to claim 57, wherein each of said sets of snoop accesses contains exactly one snoop access.

65. (new) A method for transferring a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through at least three entire L-byte lines of said secondary memory address space; and

initiating snoop accesses of said cache memory for each entire L-byte line of said transaction, said snoop accesses each specifying a respective L-byte line in its entirety, the first data unit of said transaction being read from said secondary memory before any snoop access specifying an L-byte line beyond the first entire L-byte line of said transaction is initiated,

wherein except at cache line boundaries preceding cache lines for which a snoop access returns negatively, all data units of said PCI-bus burst transaction are transferred to said bus master at a constant data rate.

66. (new) A method according to claim 65, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

67. (new) A method according to claim 66, wherein said processing unit samples snoop accesses in accordance with a first clock, and wherein said bus master samples data transferred to it in accordance with a PCI clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

68. (new) Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst read access initiated by said bus master,

sequentially transfers data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through at least three entire L-byte lines of said secondary memory address space; and

for each entire L-byte line of said transaction, initiates a respective set of at least one snoop access of said cache memory, the snoop accesses in each set collectively specifying a respective L-byte line in its entirety, all of the snoop accesses in each set being initiated early enough such that any responses to them can be sampled prior to completion of the transfer to said bus master of the first data unit in the respective specified L-byte line, the first data unit of said transaction being read from said secondary memory before any snoop access specifying any part of an L-byte line beyond the first entire L-byte line of said transaction is initiated,

wherein except at cache line boundaries preceding cache lines for which the snoop access returns negatively, all data units of said PCI-bus burst transaction are transferred to said bus master at a constant data rate.

69. (new) Apparatus according to claim 68, wherein for each given one of said data units transferred in said burst transaction, the controller apparatus circuitry:

drives said given data unit onto a PCI bus; and

asserts a target-ready signal on said PCI bus for sampling by said bus master in dependence upon a PCI-bus clock signal.

70. (new) Apparatus according to claim 69, wherein said processing unit samples snoop accesses in accordance with a first clock,

and wherein said first clock operates at at least twice the frequency of said PCI clock.

71. (new) Apparatus according to claim 68, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

72. (new) Apparatus according to claim 68, wherein all the snoop accesses in each respective set of snoop accesses initiated in said step of initiating, are initiated early enough such that they can be sampled by said host processing unit prior to completion of the transfer to said bus master of the last data unit in the respective L-byte line immediately preceding the specified L-byte line.

73. (new) Apparatus according to claim 68, wherein the set of snoop accesses collectively specifying a particular one of the L-byte lines in its entirety contains all the snoop accesses of said cache memory which are initiated in said step of transferring and which specify any part of the particular L-byte line.

74. (new) Apparatus according to claim 68, wherein each of said sets of snoop accesses contains exactly one snoop access.

75. (new) Controller apparatus for a computer system which includes a secondary memory having an address space, a bus master, a processing unit and a cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in response to a PCI-bus burst read access initiated by said bus master,

sequentially transfers data units to said bus master from said secondary memory according to a PCI-bus burst transaction, beginning at a starting memory location address in said secondary memory address space and continuing through at least three entire L-byte lines of said secondary memory address space; and

initiates snoop accesses of said cache memory for each entire L-byte line of said transaction, said snoop accesses each specifying a respective L-byte line in its entirety, the first data unit of said transaction being read from said secondary memory before any snoop access specifying an L-byte line beyond the first entire L-byte line of said transaction is initiated,

wherein except at cache line boundaries preceding cache lines for which the snoop access returns negatively, all data units of said PCI-bus burst transaction are transferred to said bus master at a constant data rate.

76. (new) Apparatus according to claim 75, wherein each full L-byte line of said transaction requires at least 8 data unit transfers to said bus master.

77. (new) A method for transferring a plurality of data units between a bus master and a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said first cache memory having a line size of L bytes, comprising the steps of:

sequentially transferring data units between said bus master and said secondary memory beginning at a starting memory location address in an N'th L-byte line of said secondary memory address space and continuing beyond an L-byte boundary of said secondary memory address space, said sequentially transferred data units including a last data unit before said L-byte boundary and a first data unit beyond said L-byte boundary;

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said step of transferring, and prior to completion of the transfer of the last data unit before said L-byte boundary, initiating a next-line inquiry to determine whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory; and

where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, beginning a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory prior to completion by the bus master of the transfer of the last data unit before said L-byte boundary.

78. (new) A method according to claim 77, wherein where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a

modified state in said first cache memory, and wherein said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion by the bus master of the transfer of the last data unit before said L-byte boundary.

79. (new) A method for reading a plurality of data units to a bus master from a respective plurality of memory locations at sequential memory location addresses in an address space of a secondary memory, for use with a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said first cache memory having a line size of L bytes, comprising the steps of:

sequentially transferring data units to said bus master from said secondary memory beginning at a starting memory location address in an N'th L-byte line of said secondary memory address space and continuing beyond an L-byte boundary of said secondary memory address space, said sequentially transferred data units including a last data unit before said L-byte boundary and a first data unit beyond said L-byte boundary;

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said step of transferring, and prior to completion of the transfer of the last data unit before said L-byte boundary, initiating a next-line inquiry to determine whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory; and

where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, beginning a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory prior to completion of the transfer to said bus master of the last data unit before said L-byte boundary.

80. (new) A method according to claim 79, wherein where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a

modified state in said first cache memory, and wherein said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion of the transfer to said bus master of the last data unit before said L-byte boundary.

81. (new) A method for transferring data between a bus master and a plurality of memory locations at respective addresses in an address space of a secondary memory, for use with a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said first cache memory having a line size of L bytes, comprising the steps of:

sequentially transferring at least three data units between said bus master and said secondary memory beginning at a first starting memory location address in an N'th L-byte line of said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space;

prior to completion of the transfer of the first data unit beyond said L-byte boundary, determining whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary; and

where said step of determining determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, beginning a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory, no earlier than the transfer of the first data unit of said N'th L-byte line and prior to completion by said bus master of the transfer of the first data unit beyond said L-byte boundary,

all of said transfers of data units in said step of sequentially transferring, occurring at a constant rate.

82. (new) A method according to claim 81, wherein where said step of determining determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion of the transfer of the first data unit beyond said L-byte boundary.

83. (new) A method according to claim 81, wherein said at least three data units includes at least two data units before said L-byte boundary.

84. (new) A method for reading data to a bus master from a plurality of memory locations at respective addresses in an address space of a secondary memory, for use with a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said first cache memory having a line size of L bytes, comprising the steps of:

sequentially transferring at least three data units to said bus master from said secondary memory beginning at a first starting memory location address in an N'th L-byte line of said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space;

prior to completion of the transfer of the first data unit beyond said L-byte boundary, determining whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary; and

where said step of determining determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, beginning a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory, no earlier than the transfer of the first data unit of said N'th L-byte line and prior to completion by said bus master of the transfer of the first data unit beyond said L-byte boundary,

all of said transfers of data units in said step of sequentially transferring, occurring at a constant rate.

85. (new) A method according to claim 84, wherein where said step of determining determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion of the transfer of the first data unit beyond said L-byte boundary.

86. (new) A method according to claim 84, wherein said at least three data units includes at least two data units before said L-byte boundary.

87. (new) A method for reading data in a burst from a memory to a PCI master in response to a burst read access by said PCI master, in a system which includes a processing subsystem having a first level cache which caches locations of said memory for said processing subsystem, said cache having a line size of L bytes, said burst read access identifying a starting address in a line N of said memory and continuing beyond an L-byte boundary, comprising the steps of:

reading data from said memory according to said burst read access;

transferring said data to said PCI master;

initiating an inquiry cycle of at least part of line N+1 in said first level cache during at least one of said steps of reading and transferring; and

where said inquiry cycle returns an indication that at least part of said line N+1 is cached modified in said first level cache, performing a write-back of said line N+1 to said memory at least partially during said step of transferring said data to said PCI master.

88. (new) A method according to claim 87, wherein said step of performing a write-back of said line N+1 to said memory completes during said step of transferring said data to said PCI master.

89. (new) Controller apparatus for a system which includes a secondary memory having an address space, a bus master, a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred with said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in performance of a burst data transfer:

sequentially transfers data units between said bus master and said secondary memory beginning at a starting memory location address in an N'th L-byte line of said secondary memory address space and continuing beyond an L-byte boundary of said secondary memory address space, said sequentially transferred data units including a last data unit before said L-byte boundary and a first data unit beyond said L-byte boundary;

no earlier than the transfer of the first data unit for each entire N'th L-byte line in burst transfer, and prior to completion of the transfer of the last data unit before said L-byte boundary, initiates a next-line inquiry to determine whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory; and

where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, begins a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory prior to completion by the bus master of the transfer of the last data unit before said L-byte boundary.

90. (new) Apparatus according to claim 89, wherein where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a

modified state in said first cache memory, and wherein said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion by the bus master of the transfer of the last data unit before said L-byte boundary.

91. (new) Controller apparatus for a system which includes a secondary memory having an address space, a bus master, a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in performance of a burst data read transfer:

sequentially transfers data units to said bus master from said secondary memory beginning at a starting memory location address in an N'th L-byte line of said secondary memory address space and continuing beyond an L-byte boundary of said secondary memory address space, said sequentially transferred data units including a last data unit before said L-byte boundary and a first data unit beyond said L-byte boundary;

no earlier than the transfer of the first data unit for each entire N'th L-byte line in said burst data read transfer, and prior to completion of the transfer of the last data unit before said L-byte boundary, initiates a next-line inquiry to determine whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory; and

where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, begins a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory prior to completion of the transfer to said bus master of the last data unit before said L-byte boundary.

92. (new) Apparatus according to claim 91, wherein where said next-line inquiry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a

modified state in said first cache memory, and wherein said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion of the transfer to said bus master of the last data unit before said L-byte boundary.

93. (new) Controller apparatus for a system which includes a secondary memory having an address space, a bus master, a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred with said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in performance of a burst data transfer:

sequentially transfers at least three data units between said bus master and said secondary memory beginning at a first starting memory location address in an N'th L-byte line of said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space;

prior to completion of the transfer of the first data unit beyond said L-byte boundary, determines whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary; and

where said circuitry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, begins a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory, no earlier than the transfer of the first data unit of said N'th L-byte line and prior to completion by said bus master of the transfer of the first data unit beyond said L-byte boundary,

all of said transfers of data units of said burst transfer occurring at a constant rate.

94. (new) Apparatus according to claim 93, wherein where said circuitry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion of the transfer of the first data unit beyond said L-byte boundary.

95. (new) Controller apparatus for a system which includes a secondary memory having an address space, a bus master, a processing unit and a first cache memory which caches memory locations of said secondary memory for said processing unit, said cache memory having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said bus master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in performance of a burst data read transfer:

sequentially transfers at least three data units to said bus master from said secondary memory beginning at a first starting memory location address in an N'th L-byte line of said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary memory address space;

prior to completion of the transfer of the first data unit beyond said L-byte boundary, determines whether at least part of an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary; and

where said circuitry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, begins a write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory, no earlier than the transfer of the first data unit of said N'th L-byte line and prior to completion by said bus master of the transfer of the first data unit beyond said L-byte boundary,

all of said transfers of data units of said burst transfer occurring at a constant rate.

96. (new) Apparatus according to claim 95, wherein where said circuitry determines that at least part of said N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory, said write-back of data from said N+1'th L-byte line of said first cache memory to said secondary memory completes prior to completion of the transfer of the first data unit beyond said L-byte boundary.

97. (new) Controller apparatus for a system which includes a memory having an address space, a PCI master, a processing subsystem and a first level cache which caches memory locations of said memory for said processing subsystem, said first level cache having a line size of L bytes, and each data unit having a size equal to the largest size that can be transferred to said PCI master in parallel, said controller apparatus comprising circuitry which in a mode of operation, in performance of a burst data read access:

reads data from said memory according to said burst read access;

transfers said data to said PCI master;

initiates an inquiry cycle of at least part of line N+1 in said first level cache during at least one of said acts of reading and transferring; and

where said inquiry cycle returns an indication that at least part of said line N+1 is cached modified in said first level cache, performs a write-back of said line N+1 to said memory at least partially during said act of transferring said data to said PCI master.

98. (new) Apparatus according to claim 97, wherein the write-back of said line N+1 to said memory completes during the transfer of said data to said PCI master.